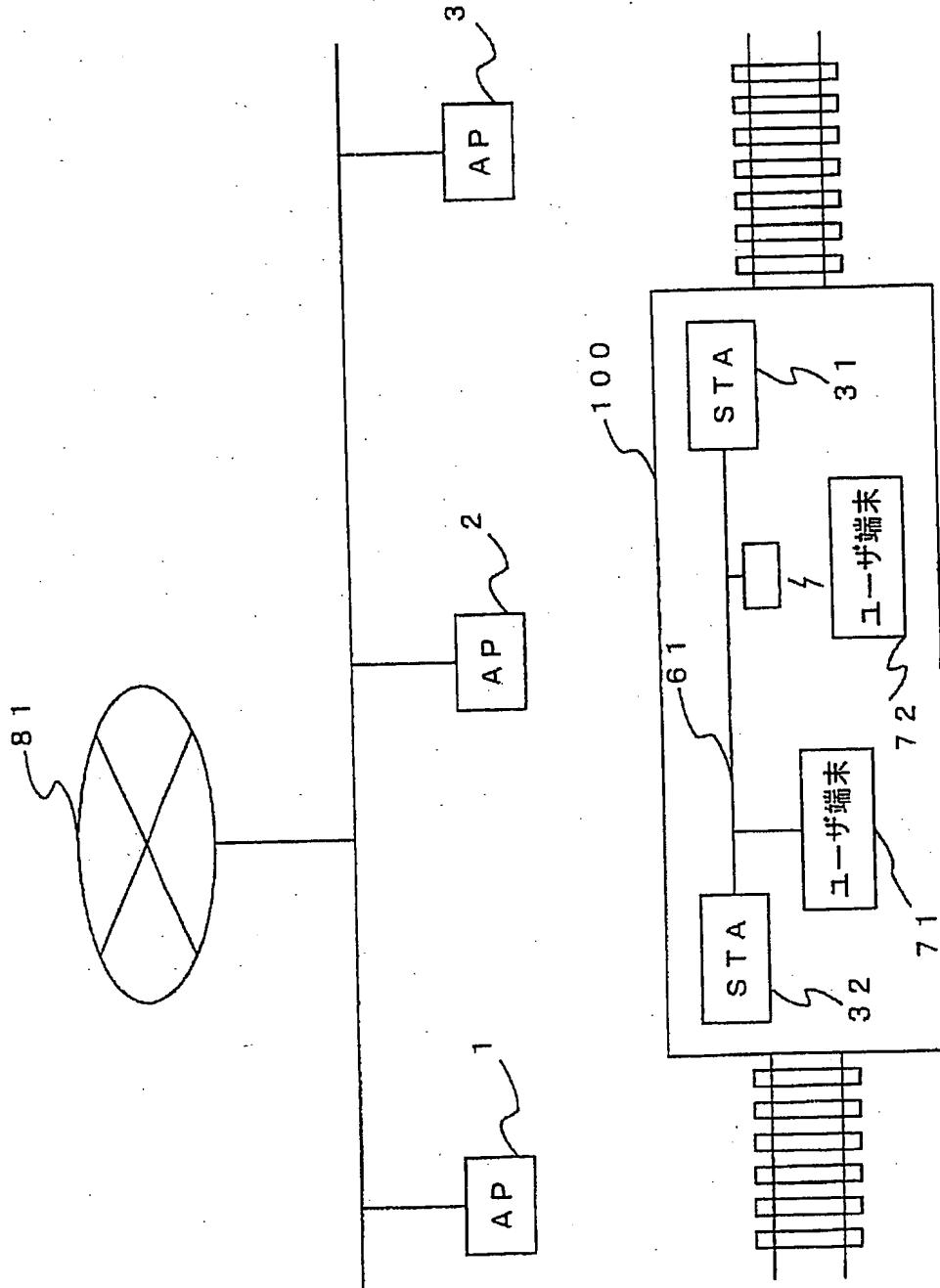


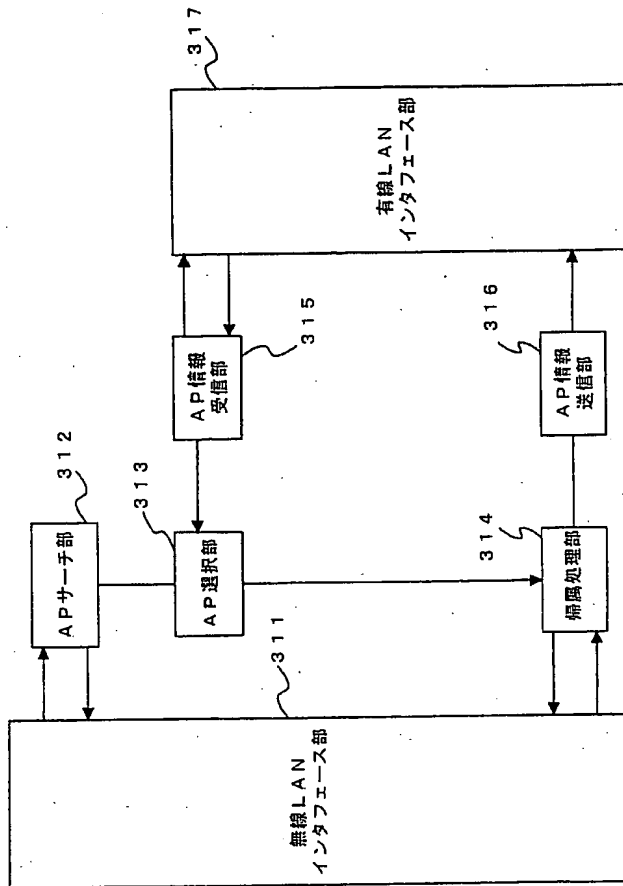
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[図1]

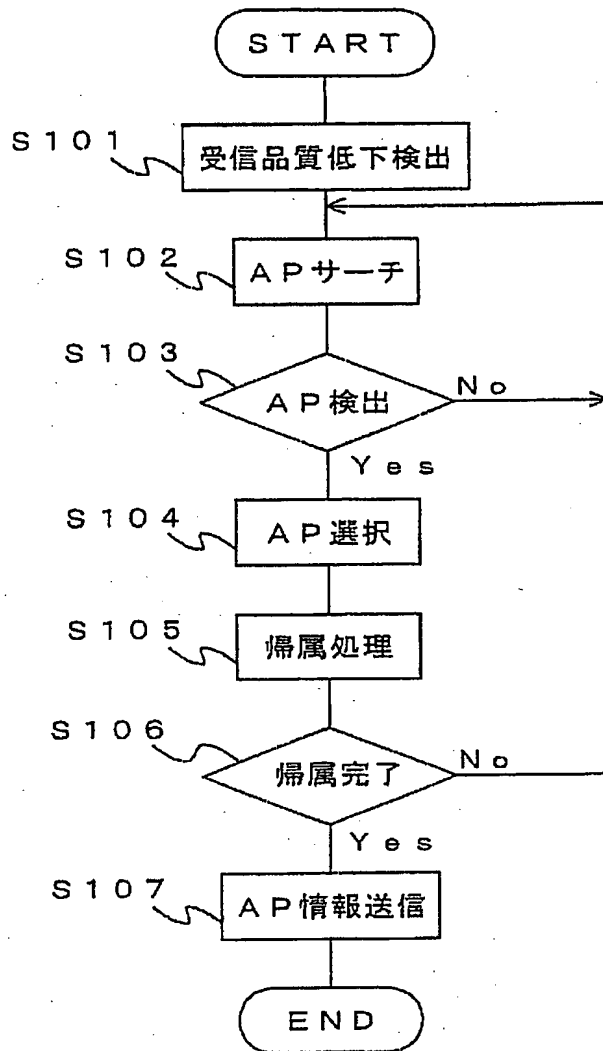


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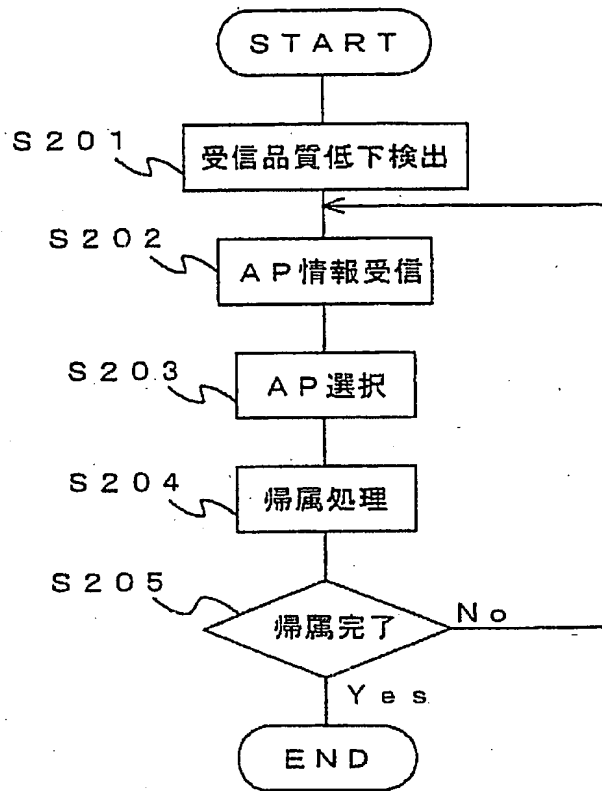
[図2]



[図3]

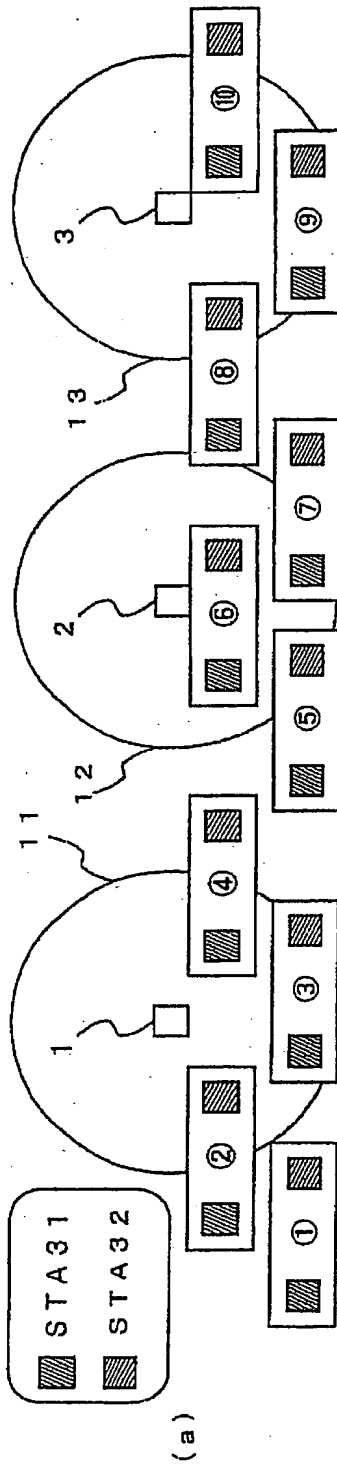


[図4]



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[図5]



(b)

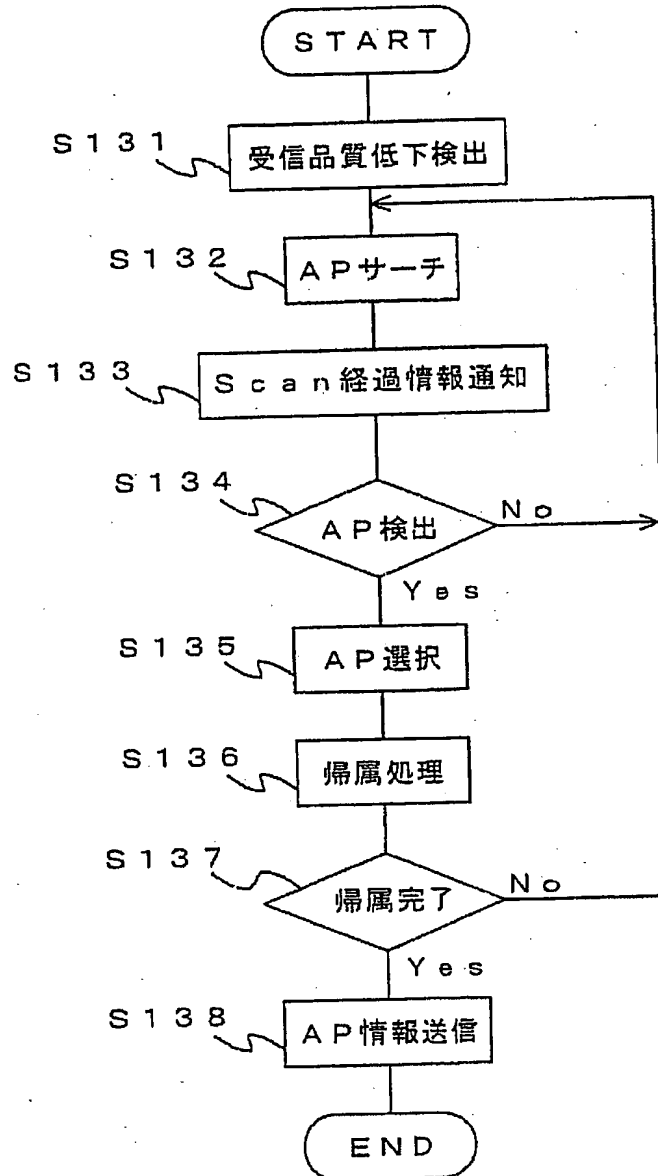
本発明	3 1	31→32	3 2
①	Scan	-	Scan
②	Scan→AP1	-	Scan
③	AP1	-	Scan→AP1
④	Scan	-	AP1
⑤	Scan→AP2	-	Scan
⑥	AP2	-	Scan→AP2
⑦	Scan	-	AP2
⑧	Scan→AP3	-	Scan
⑨	AP3	-	Scan→AP3
⑩	Scan	-	AP3

(c)

従来	3 1	31→32	3 2
①	Scan	-	Scan
②	Scan→AP1	-	Scan
③	AP1	-	Scan→AP1
④	Scan	-	AP1
⑤	Scan→AP2	-	Scan
⑥	AP2	-	Scan→AP2
⑦	Scan	-	AP2
⑧	Scan→AP3	-	Scan
⑨	AP3	-	Scan→AP3
⑩	Scan	-	AP3

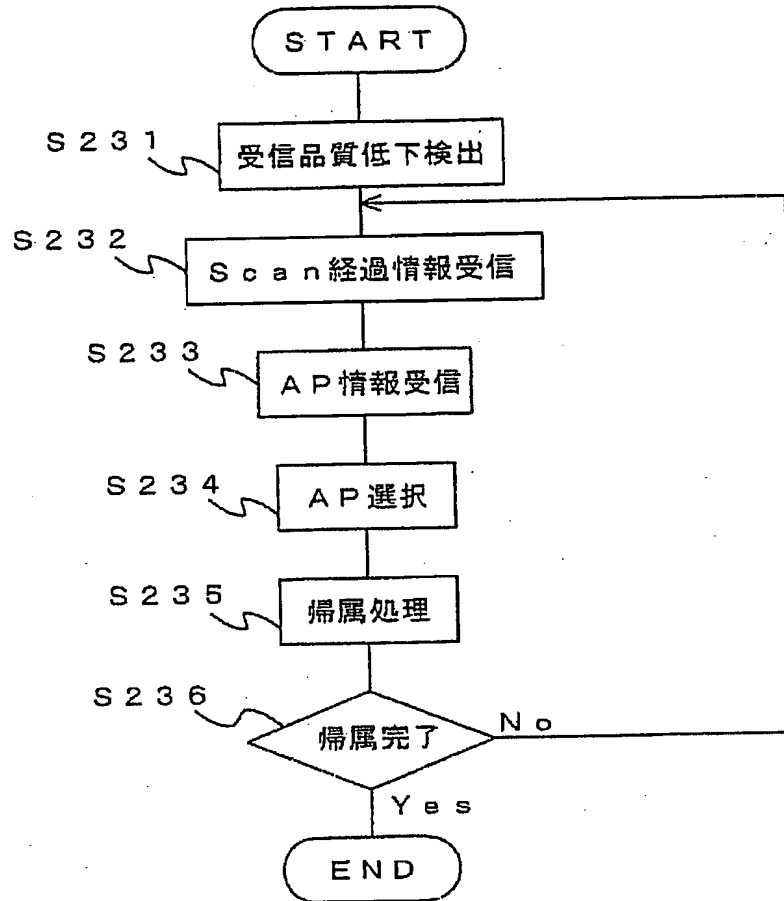
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[図6]

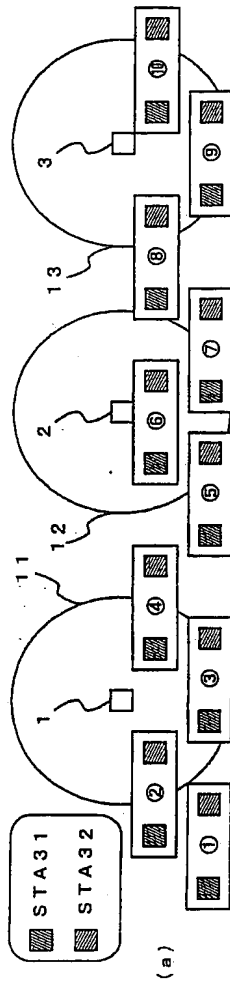


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[図7]



[図8]



本発明	31	31~32	32
①	Scan all	f1~fa: x	Scan fa+1~f14
②	Scan all→AP1	f1~f5: x	Scan f6~f14→AP1
③			
④	Scan all	f1~fb: x	AP1
⑤			
⑥	Scan all→AP2	f1~f8: x	Scan f9~f14→AP2
⑦	Scan all		AP2
⑧			
⑨	Scan all→AP3	AP3	AP3
⑩	Scan all	f1~fc: x	AP2

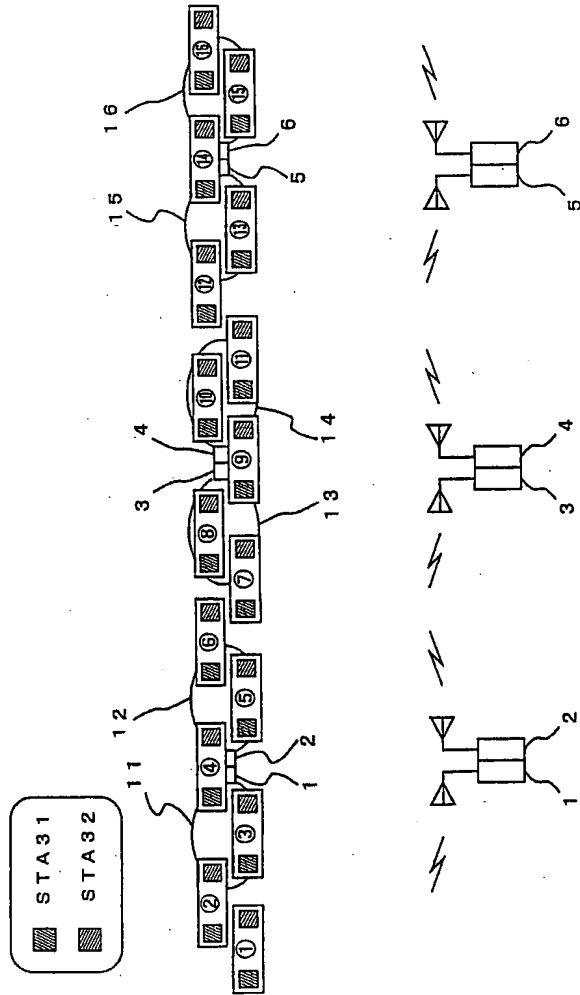
The diagram illustrates the internal structure and data flow of two stations, STA 31 and STA 32.

STA 31: This station consists of a vertical column of 14 data registers labeled f 1 through f 14. To the right of these registers is a large rectangular block representing control logic. This block has multiple inputs from the registers, with specific connections indicated by lines and 'x' marks. For example, lines from f 1, f 2, f 3, f 4, and f 5 connect to the top of the block, while lines from f 6, f 7, f 8, f 9, f 10, f 11, f 12, f 13, and f 14 connect to the bottom. A horizontal line of dots between f 7 and f 8 indicates that the pattern of connections continues for the intermediate registers.

STA 32: This station also features a vertical column of 14 data registers labeled f 1 through f 14. To the right of these registers is another large rectangular block representing control logic. This block has inputs from the registers, with lines from f 1, f 2, f 3, f 4, f 5, and f 6 connecting to the top, and lines from f 7, f 8, f 9, f 10, f 11, f 12, f 13, and f 14 connecting to the bottom. A horizontal line of dots between f 7 and f 8 indicates that the pattern of connections continues for the intermediate registers. Additionally, there is a feedback loop from the output of the control logic block back to the input of the f 1 register, indicated by a line with an arrow.

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[図10]



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[図11]

本発明	3 1	31→32	3 2
①	Scan	—	—
②	Scan→AP1	AP1	—
③	AP1	—	AP1
④	Scan→AP2	AP2	AP1
⑤	AP2	—	AP2
⑥	Scan	—	AP2
⑦	Scan→AP3	AP3	—
⑧	AP3	—	AP3
⑨	Scan→AP4	AP4	AP3
⑩	AP4	—	AP4
⑪	Scan	—	AP4
⑫	Scan→AP5	AP5	—
⑬	AP5	—	AP5
⑭	Scan→AP6	AP6	AP5
⑮	AP6	—	AP6
⑯	Scan	—	AP6

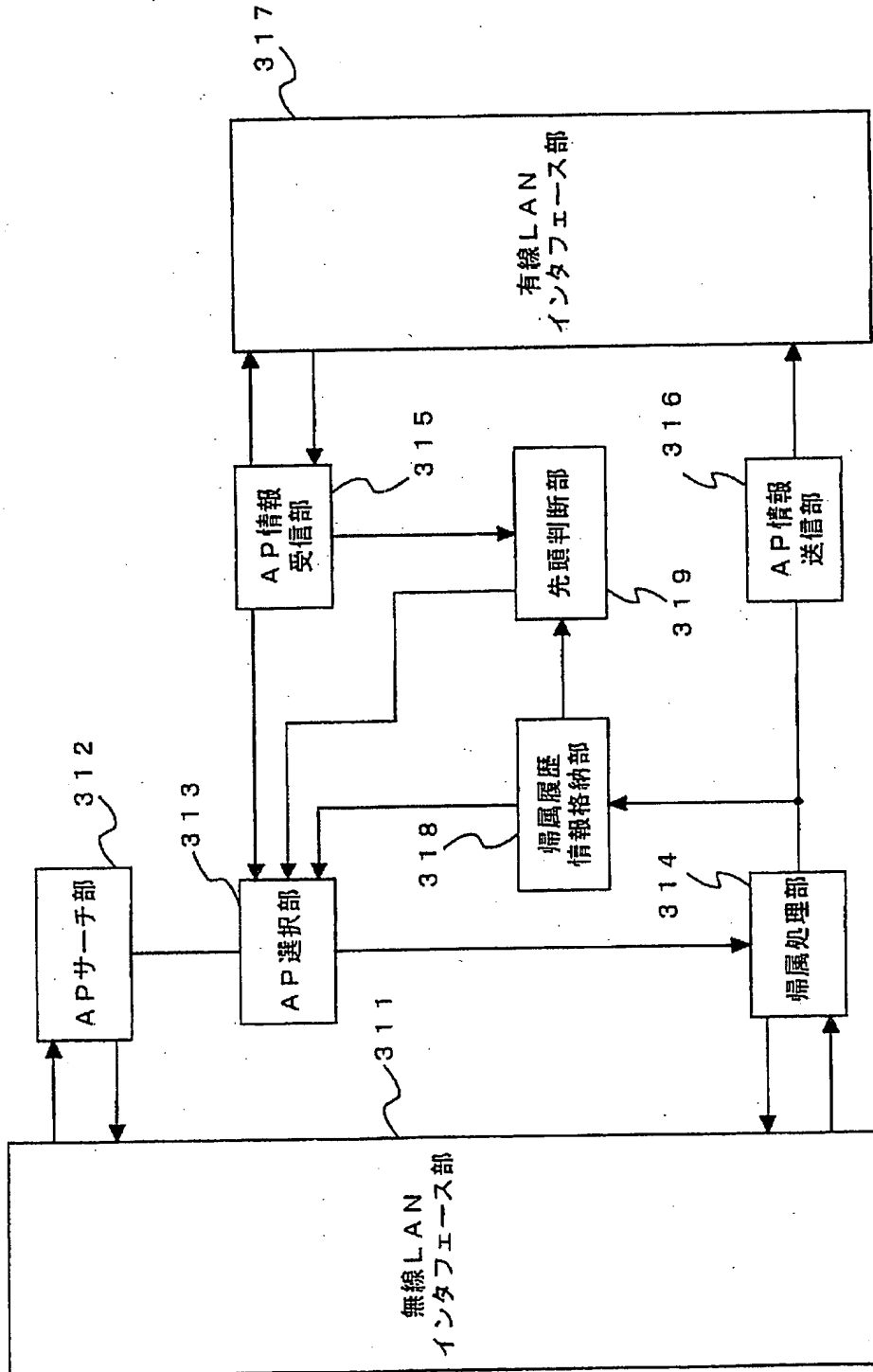
(a)

従来	3 1	31→32	3 2
①	Scan	—	Scan
②	Scan→AP1	—	Scan
③	AP1	—	Scan→AP1
④	Scan→AP2	—	AP1
⑤	AP2	—	Scan→AP2
⑥	Scan	—	AP2
⑦	Scan→AP3	—	Scan
⑧	AP3	—	Scan→AP3
⑨	Scan→AP4	—	AP3
⑩	AP4	—	Scan→AP4
⑪	Scan	—	AP4
⑫	Scan→AP5	—	Scan
⑬	AP5	—	Scan→AP5
⑭	Scan→AP6	—	AP5
⑮	AP6	—	Scan→AP6
⑯	Scan	—	AP6

(b)

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[図12]



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[図13]

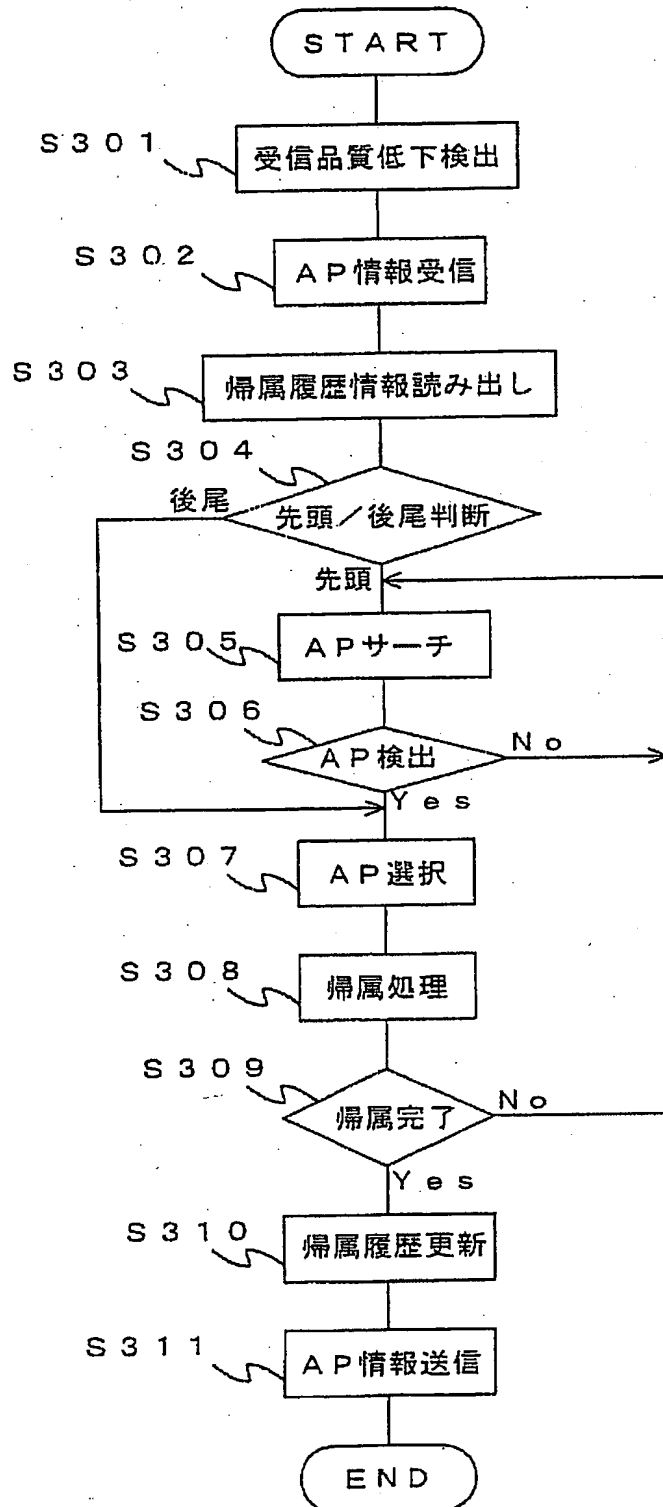
No.	AP識別子	周波数
1	AP5	f1
2	AP4	f14
3	AP3	f11
4	AP2	f6
5	AP1	f1

(a) 帰属履歴情報

No.	AP識別子	周波数
1	AP6	f6
2	AP5	f1
3	AP4	f14
4	AP3	f11
5	AP2	f6
6	AP1	f1

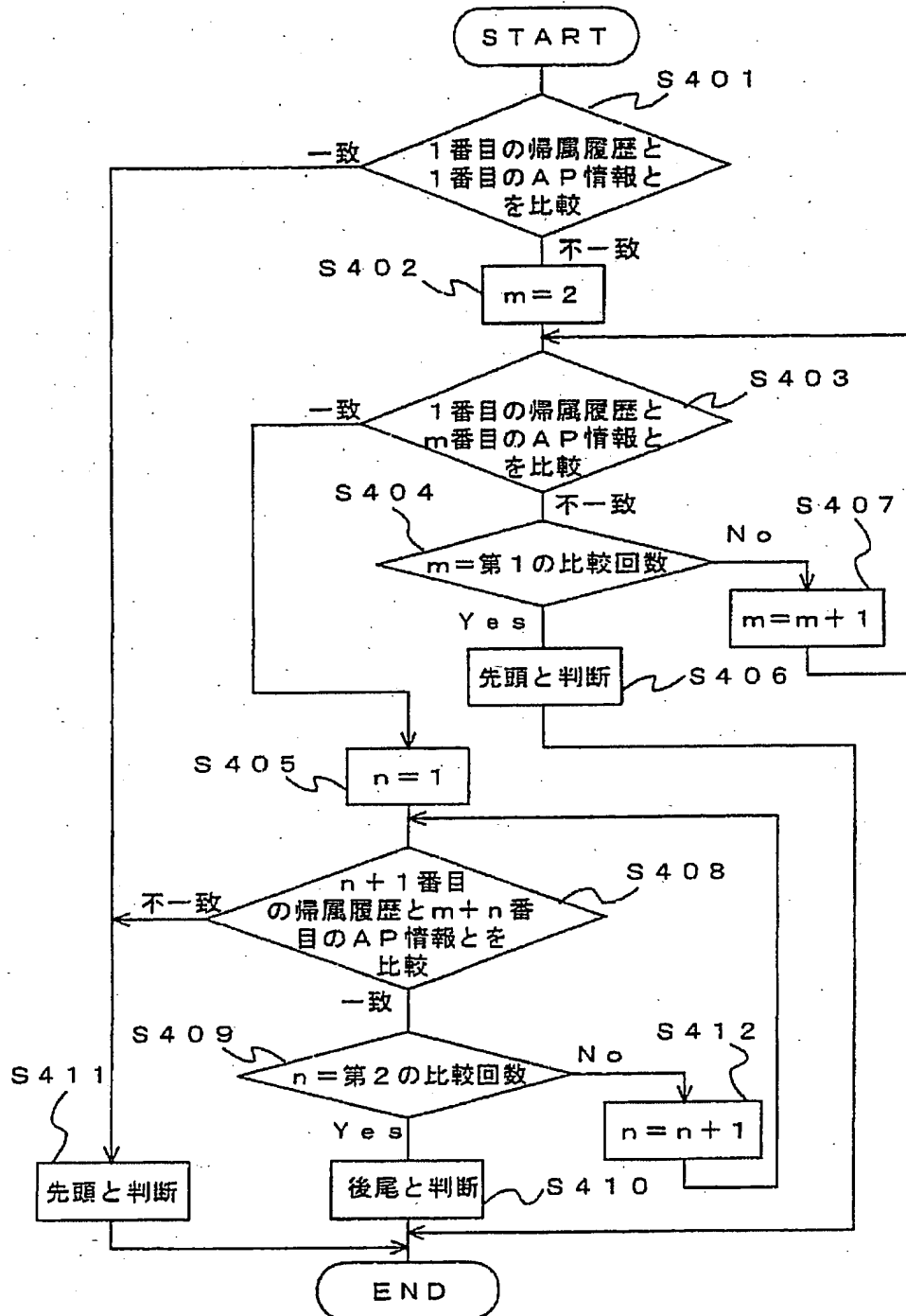
(b) AP情報

[図14]



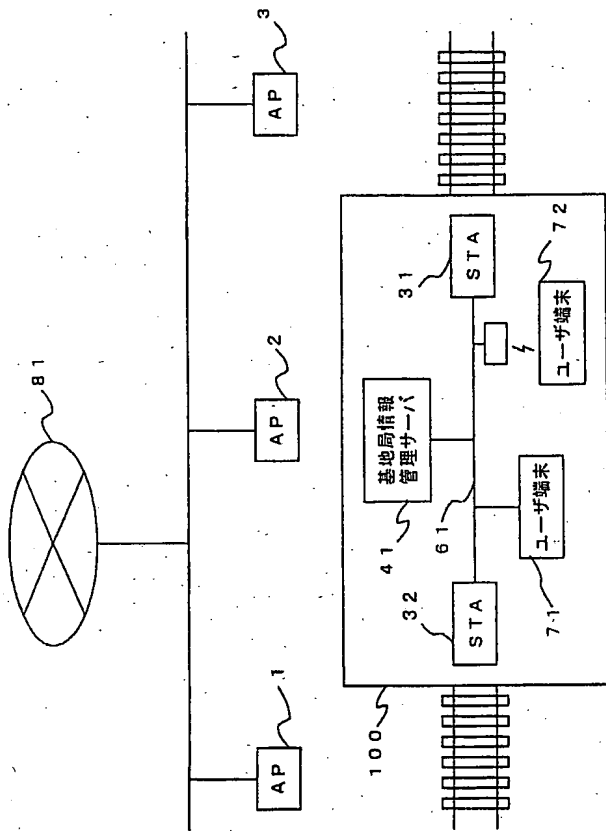
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[図15]



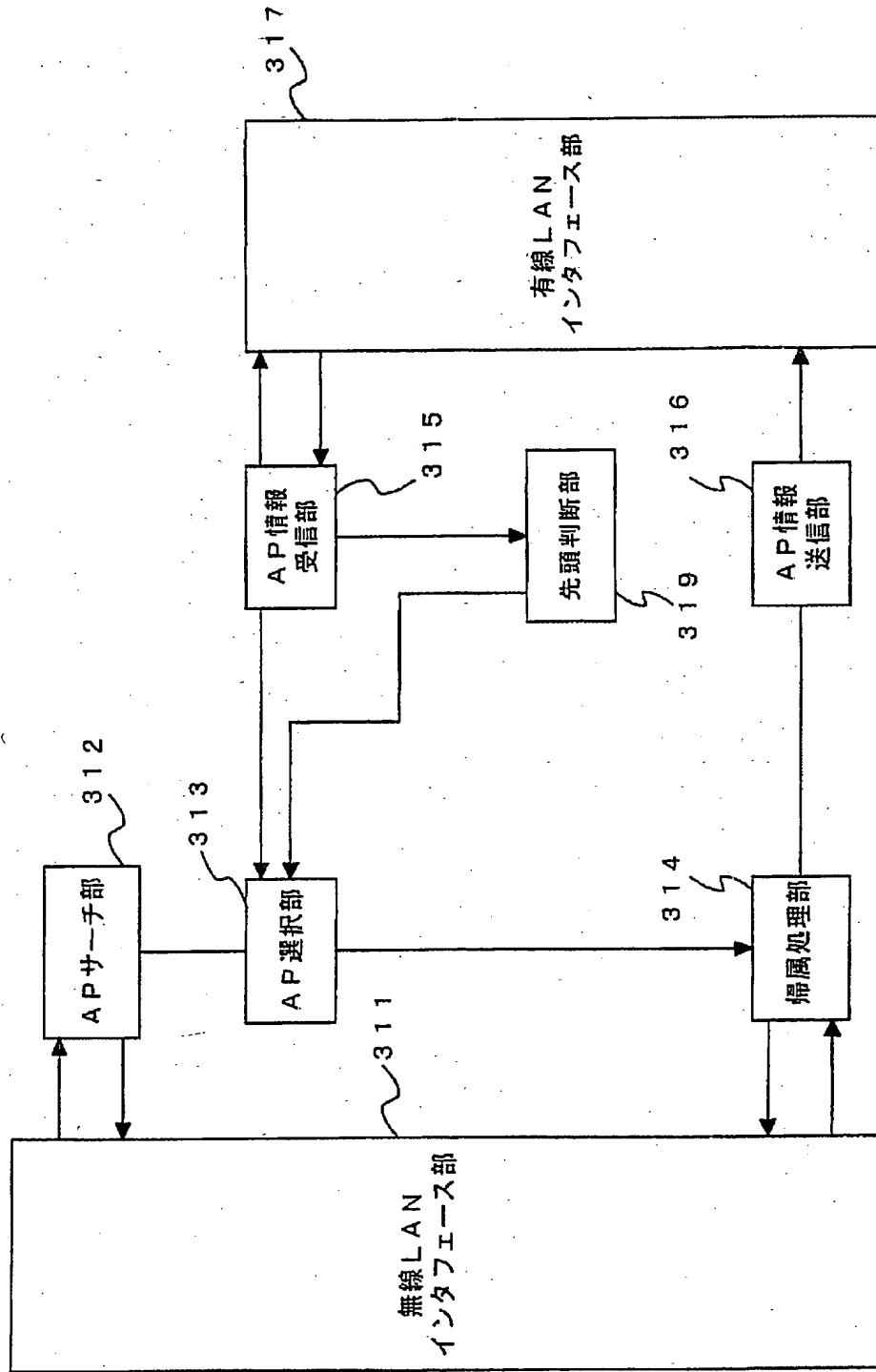
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[図16]

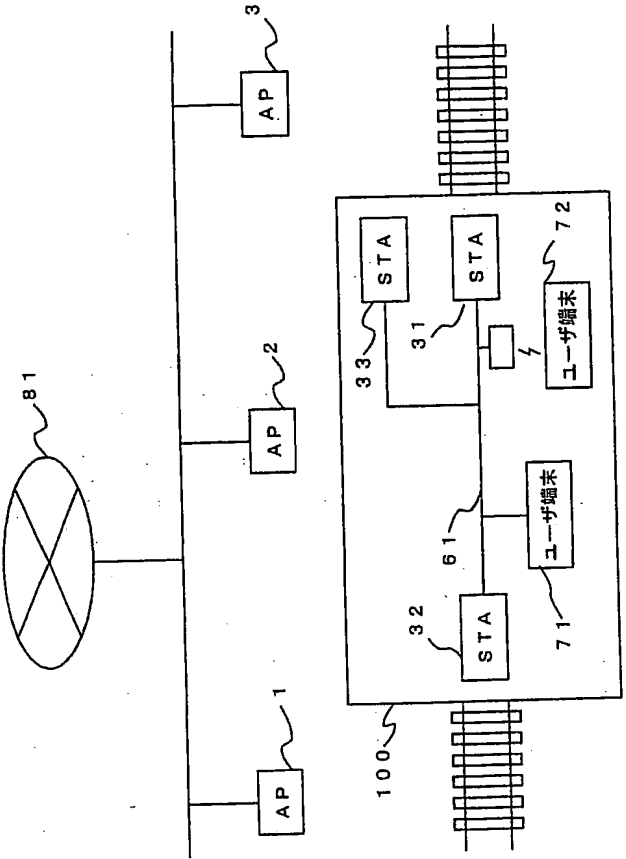


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[図17]

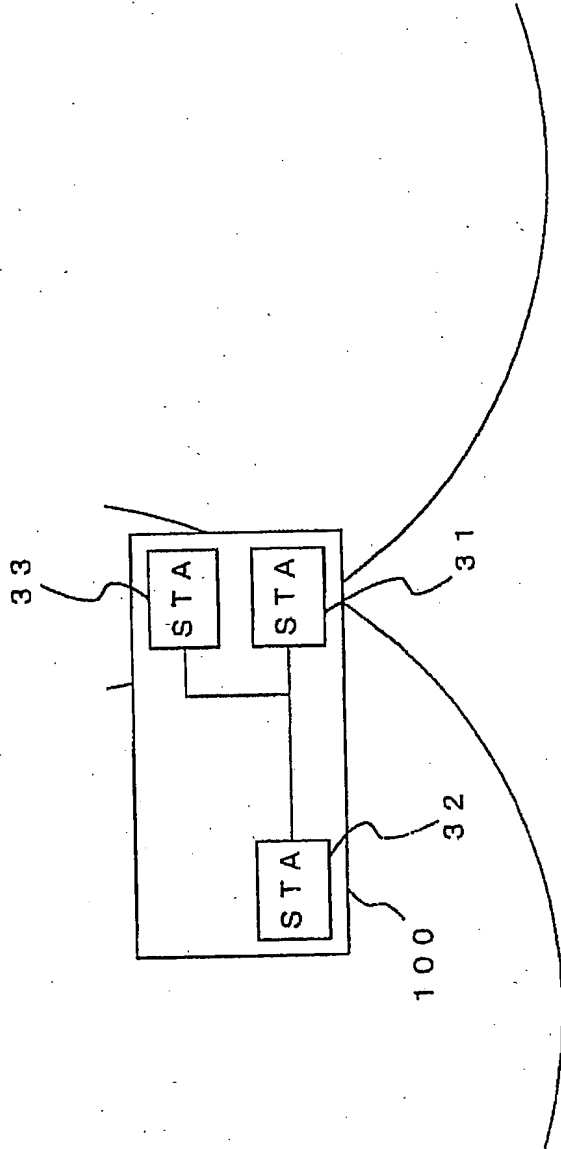


[図18]



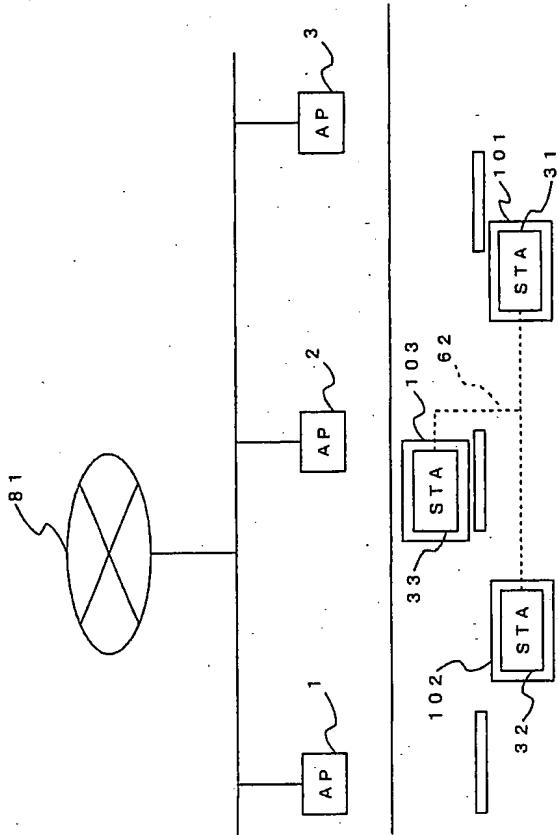
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[図20]



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[図21]

